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	Application No.	Applicant(s)
Notice of Allowability	10/026,246	BECKER, SCOTT T.
	Examiner	Art Unit
	Fred Ferris	2128
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT F of the Office or upon petition by the applicant. See 37 CFR 1.31	S (OR REMAINS) CLOSED in th b) or other appropriate communic RIGHTS. This application is subj	is application. If not included
1. This communication is responsive to <u>7 April 2005.</u>		
2. The allowed claim(s) is/are <u>1-14</u> .		
3. X The drawings filed on 1 November 2004 are accepted by the Examiner.		
4.		
Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Sumr Paper No./Ma 08), 7. ☐ Examiner's Am	il Date
U.S. Patent and Trademark Office PTOL-37 (Rev. 1-04)	otice of Allowability	Part of Paper No./Mail Date 04212005

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DETAILED ACTION

1. This Office Action is in response to applicants after final amendment filed 7 April 2005. Claims 1-14 have now been allowed over the prior art of record.

Response to Arguments

2. Applicant's arguments filed on 7 April 2005 with respect to claims 1-14 have been fully considered and found to be persuasive.

Regarding applicant's response to obviousness-type double patenting rejection:

The examiner withdraws the obviousness type double patenting rejection of claims 1-14 over copending application No. 10/026,245 in view of applicant's Terminal Disclaimer filed 7 April 2005. This being the only outstanding issue pending from the final office action of 28 March 2005, the case is now in condition for allowance.

Allowable Subject Matter

3. Claims 1-14 have been allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a method of designing a memory device design with reduced bitline capacitance offsets inclusive of a memory core having a depth that defines multiple words and a word width defined by multiple pairs of global bitlines and global complementary bitlines. This has been disclosed in the prior art of record.

While these features are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

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"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In particular, the prior art of record does not disclose the specific arrangement of elements where "a core cell (defined as six transistor cell, Fig. 3A) having bitlines and complementary bitlines" includes a "flipped core cell that has a flipped bitlines and a flipped complementary bitline, with "multiple pairs of the global bitlines and the global complementary bitlines" (i.e. a rotation of the core cell about its axes and coupling pairs of core cells, Figs. 2A, 3B, to achieve a reduction in the bitline capacitance offsets), as now recited in independent claims 1 and 12, in the context of the claims. Claims 2-11 and 13-14 are allowable as being dependent from independent claims 1 and 12 respectively.

The closest prior art uncovered during examination is:

<u>US Patent 5,999,482 issued to Kornachuk et al</u>: teaches a memory core design having a model word-line defining the memory core configuration.

<u>US Patent 6,043,562 issued to Keeth</u>: discloses a semiconductor memory with multiple layers and offset conductive levels with cross-coupled transistor pairs.

While the prior art of record discloses various arrangements of core cells including six transistor core cells having a bitline and complementary bitline for reducing capacitances and a depth of memory defined by the number of wordlines, it does not

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explicitly disclose the specific arrangement of elements relating to "a core cell (defined as six transistor cell, Fig. 3A) having a bitline and complementary bitline" including a "flipped cores cell that has a flipped bitline and a flipped complementary bitline, with "multiple pairs of the global bitline and the global complementary bitline", as now recited in independent claims 1 and 12. (See: Figs. 2A-3A) This feature renders the claimed invention non-obvious over the prior art of record.

Conclusion

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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